EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	3419	716/8-11,16.ccls.	US-PGPUB; USPAT	OR	ON	2007/05/06 17:02
L9	129869	("PLD" "FPGA" "PAL" "PLA" programmable adj (logic array))	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:02
L10	597536	(cluster$3 group$4 pack$4 mapping) same (block cell logic)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:03
L11	852126	(placing placement) and (arrang$5 re$arrang$5 re$locat$4 re$posit$4 swap$4 permut$6 remov$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:04
L12	36199	L9 and L10	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:04
L13	10479	L11 and L12	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:04
L14	82907	design near5 (rule constraint restrict$4 specification)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:06
L15	1261	L13 and L14	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:05

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L16	162	L8 and L15	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:05
L17	53	L16 and attribut$4	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:06
L18	6390	design near5 (rule constraint restrict$4 specification) same (timing rout$6 pin)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:07
L19	45	L17 and L18	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/05/06 17:07

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	0	716/8-11,16.ccls. and (("PLD" "FPGA" "PAL" "PLA" programmable adj (logic array)) and (placing placement) and (cluster$3 group$4 pack$4 mapping) and (block cell logic) and (arrang$5 re$arrang$5 re$locat$4 re$posit$4 swap$4 permut$6 remov$4) and design adj (rule constraint restrict$4 specification)).clm.	US-PGPUB; USPAT	OR	ON	2007/05/06 16:58
L7	0	(("PLD" "FPGA" "PAL" "PLA" programmable adj (logic array)) and (placing placement) and (cluster$3 group$4 pack$4 mapping) and (block cell logic) and (arrang$5 re$arrang$5 re$locat$4 re$posit$4 swap$4 permut$6 remov$4) and design adj (rule constraint restrict$4 specification)).clm.	US-PGPUB; USPAT	OR	ON	2007/05/06 16:58